

MPEG AUDIO / MPEG-2 VIDEO INTEGRATED DECODER**BRIEF DATA**

- SINGLE CHIP COMBINING THE DECODING FUNCTIONS OF THE STi3500A VIDEO DECODER AND THE STi4500 AUDIO DECODER
- ON-CHIP PLL ALLOWING FULL CHIP OPERATION WITH TWO EXTERNAL CLOCKS
- VIDEO DECODER FULLY SUPPORTS MPEG-2 MAIN PROFILE/MAIN LEVEL (MP@ML)
- AUTOMATIC VIDEO ERROR CONCEALMENT
- ENHANCED ON-SCREEN DISPLAY GENERATOR : 16 COLORS/REGION, LINKED LIST MEMORY MANAGEMENT
- AUDIO DECODER SUPPORTS LAYERS I & II OF MPEG
- ALL POPULAR PCM AUDIO OUTPUT FORMATS SUPPORTED
- STANDARD 8-BIT INTERFACE FOR MICROCONTROLLER AND COMPRESSED DATA INPUT
- 3.3V POWER SUPPLY, I/Os 5V TTL COMPATIBLE
- 0.5µm CMOS TECHNOLOGY

APPLICATIONS

- DBS RECEIVER
- DIGITAL TV RECEIVER
- DIGITAL CABLE TV RECEIVER

DESCRIPTION

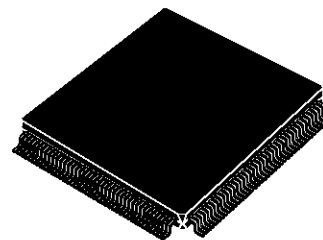
The video decoder is a real-time video decompression processor supporting the MPEG-1 and MPEG-2 standards at video rates up to 720 x 480 x 60Hz or 720 x 576 x 50Hz. Picture format conversion for display is performed by a vertical and a horizontal filter (sample rate converter). External DRAM, typically of size 16 Mbits is required.

The audio decoder is compliant with layers I and II of the MPEG standard. Sampling rates of 32, 44.1 and 48kHz can be used.

The STi3520 requires minimal support from an external microcontroller, which is mainly required to initialise the video decoder at the start of every picture. Separate audio and video data streams are input through the 8-bit data port. Time stamps are detected and made available to the microcontroller for the management of audio/video synchronization.

User-defined bitmaps may be superimposed on the displayed picture through use of the on-screen display function. These bitmaps are written directly into the DRAM memory by the microcontroller.

Undetected bitstream errors which would cause decoder errors activate the error concealment functions.



PQFP160
(Plastic Quad Flat Pack)

ORDER CODE : STi3520CV